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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,334	02/09/2004	Toshiyuki Kasai	118378	8924

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EXAMINER	
NGUYEN, JENNIFER T	
ART UNIT	**PAPER NUMBER**
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/773,334	KASAI, TOSHIYUKI	
	Examiner	Art Unit	
	Jennifer T. Nguyen	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/9/04;1/30/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 4, 6, and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Maede et al. (Patent No.: US 6,756,738).

Regarding claims 1 and 4, Maede teaches a current generating circuit (fig. 5), comprising:

a power supply terminal having a power supply voltage (V+) applied thereto;

a first resistor (one resistor) and a second resistor (two resistors connect in series) (fig. 5), one end of each of the first resistor and the second resistor being coupled to the power supply terminal, and a resistance of the first resistor and a resistance of the second resistor being different.

a first transistor (shown in fig. 5) that allows a current corresponding to a voltage of a gate of the first transistor to flow between a first terminal and a second terminal of the first transistor, the first terminal being coupled to another end of the first resistor, and the second terminal and the gate being coupled with each other; and

a second transistor (shown in fig. 5) that allows a current corresponding to a voltage of a gate of the second transistor to flow between a first terminal and a second terminal of the second

transistor, the first terminal being coupled to another end of the second resistor, and the gate of the second transistor being coupled to the gate of the first transistor (col. 2, lines 14-40).

Regarding claim 6, Maede teaches a plurality of the current generating circuits are cascade-connected, and the current flowing in the second transistor of the current generating circuit disposed at a first stage is allowed to flow in the first transistor of the current generating circuit disposed at a second stage (fig. 6, col. 2, lines 41-67).

Regarding claim 7 , Maede teaches a D/A conversion circuit that converts digital data into a current signal indicating a current corresponding to digital data and that allows the current signal to flow in the first transistor (fig. 6, col. 2, lines 41-67).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 3, 5, and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maede et al. (Patent No.: US 6,756,738) in view of Kim et al. (Patent No.: US 6,633,136).

Regarding claims 2 and 3, Maede teaches all the limitations except at least one of the first resistor and the second resistor being a variable resistor.

Kim teaches a resistor (VR) connect a second transistor (Qp1) is a variable resistor (fig. 2, col. 2, lines 10-31). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the variable resistor as taught by Kim in the

system of Maede in order to allow adjusting the output current of the current generating circuit easily.

Regarding claim 5, although the combination of Maede and Kim does not specifically teach the variable resistor being configured such that a plurality of resistor devices is having predetermined resistances are coupled in parallel with each other. However, it would have been obvious to obtain a plurality of resistor devices having predetermined resistances are coupled in parallel with each other in order to allow adjusting the output current of the current generating circuit easily.

Regarding claim 16, Maede teaches a plurality of the current generating circuits are cascade-connected, and the current flowing in the second transistor of the current generating circuit disposed at a first stage is allowed to flow in the first transistor of the current generating circuit disposed at a second stage (fig. 6, col. 2, lines 41-67).

Regarding claims 17 , Maede teaches a D/A conversion circuit that converts digital data into a current signal indicating a current corresponding to digital data and that allows the current signal to flow in the first transistor (fig. 6, col. 2, lines 41-67).

Regarding claim 18, in different embodiment (fig. 3a), Maede teaches an electro-optical apparatus, comprising:

pixel circuits (20) disposed at intersections of a plurality of scanning lines and a plurality of data lines;

a scanning-line drive circuit (17) that selects the scanning lines; and

a data-line drive circuit (100) including the current generating circuit set forth in claim 1, and that supplies a current flowing in the second transistor of the current generating circuit to the data lines,

the pixel circuit, disposed at the intersection between one scanning line and one data line, comprising:

a capacitor device (C) that stores electrical charge in accordance with the current flowing in the data line when the scanning line is selected by the scanning-line drive circuit; and

an electro-optical device (21) in which a current corresponding to an electrical charge stored in a capacitor device flows when selection of the scanning line is finished (col. 8, line 41 to col. 9, line 25).

5. Claims 8, 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maede et al. (Patent No.: US 6,756,738).

Regarding claim 8, in different embodiment (fig. 3a), Maede teaches an electro-optical apparatus, comprising:

pixel circuits (20) disposed at intersections of a plurality of scanning lines and a plurality of data lines;

a scanning-line drive circuit (17) that selects the scanning lines; and

a data-line drive circuit (100) including the current generating circuit set forth in claim 1, and that supplies a current flowing in the second transistor of the current generating circuit to the data lines,

the pixel circuit, disposed at the intersection between one scanning line and one data line, comprising:

a capacitor device (C) that stores electrical charge in accordance with the current flowing in the data line when the scanning line is selected by the scanning-line drive circuit; and

an electro-optical device (21) in which a current corresponding to an electrical charge stored in a capacitor device flows when selection of the scanning line is finished (col. 8, line 41 to col. 9, line 25).

Regarding claim 13, Maede teaches a memory (inherent in MPU) that stores digital data defining a grayscale of the electro-optical device; a control circuit that reads the digital data from the memory; and a D/A conversion circuit that converts the digital data read by the control circuit into a current signal indicating a current corresponding to the digital data, and for allowing the current signal to flow in the first transistor of the current generating circuit (col. 7, lines 15-40).

Regarding claim 14, Maede teaches the electro-optical device being an organic electro luminescence device (abstract).

Regarding claim 15, Maede teaches DVD player or a PDA comprising the electro-optical apparatus (col. 1, lines 28-30).

6. Claims 9 and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maede et al. (Patent No.: US 6,756,738) in view of Kasai (Patent No.: US 7,102,600).

Regarding claim 9, Maede different from claim 9 in that he does not specifically teach a plurality of types of pixel circuits corresponding to a plurality of primary colors and a data-line drive circuit including the current generating circuit for each of the primary colors, and that supplies a current flowing in the second transistor of the current generating circuit corresponding to one primary color to a data line corresponding to the primary color.

Kasai teaches a plurality of types of pixel circuits corresponding to a plurality of primary colors (10R, 10G, and 10B) and a data-line drive circuit (4) including the current generating circuit (4aR, 4aG, and 4aB) for each of the primary colors, and that supplies a current flowing in the second transistor of the current generating circuit corresponding to one primary color to a data line corresponding to the primary color (figs. 13 and 16, col. 15; line 60 to col. 16, line 22). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the plurality of types of pixel circuits corresponding to a plurality of primary colors and the current generating circuit for each of the primary colors as taught by Kasai in the system of Maede in order to avoid problem of luminance variation, since there is difference in sensitivity between red, green, and blue pixels.

Regarding claims 10-12, the combination of Maede and Kasai teaches a setting circuit that sets a resistance of the first resistor or the second resistor of the current generating circuit to a desired value (col. 10, lines 46-58).

7. The prior art made of record and not relied upon is considered to pertinent applicant's disclosure: Patent. No. US 4,446,419 and 5,926,062.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer T. Nguyen whose telephone number is 571-272-7696. The examiner can normally be reached on Mon-Fri: 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard A. Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer Nguyen
3/18/07

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